Electronic Version
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Claims

[c1] 1.A high speed data rate converting and switching circuit for use in computer memory systems comprising n memory banks, and further comprising a first external clock having a first frequency and a second external clock having a second frequency equal to n times the first frequency, the circuit comprising:
(a)a data MUX and latch subsystem which transfers each of a multiplicity of system bus data signals having the second frequency to a memory bank data signal having the first frequency during a write operation, and which transfers each of a multiplicity of memory bank data signals having the first frequency to a system data bus data signal having the second frequency during a read operation.

[c2] (b)A strobe MUX and latch subsystem which generates a memory bank strobe signal having the first frequency, and which is synchronized to the memory bank data signals with a 90 degree phase shift during the write operation , and which generates a system bus strobe signal having the second frequency which is synchronized to, and in phase with, the system bus data signals during

the read operation.

[c3] (c)a mask MUX and latch subsystem which generates a memory bank mask signal having the first frequency, and is synchronized to the memory bank data signals during the write operation .

[c4] 2.The high speed data rate converting and switching circuit of claim 1, further comprising:
(a) a multiplicity of latching circuits which increase the duration of each data bit during both the read and the write operation;
(b) means to generate an internal clock signal at the second frequency; and
(c) means to AND the internal clock signal with the output of each latching circuit,
so that the system bus data signal is at the second frequency.

[c5] 3. The high speed data rate converting and switching circuit of claim 2, further comprising means to AND the first signal with the output of each latching circuit during the read operation,
so that the memory data bank signal is synchronized with the first external clock.

[c6] 4. The high speed data rate converting and switching

circuit of claim 3, wherein the means to generate the internal clock signal at the second frequency further comprises an m-bit counter.

[c7] 5. The high speed data rate converting and switching circuit of claim 4, further comprising generating system strobe signals by ANDing a pull-up signal with the internal clock, and by ANDing a pull-down signal with the internal clock during the read operation.

[c8] 6. The high speed data rate converting and switching circuit of claim 5, wherein the internal clock generation circuit further provides a circuit which is triggered by the falling edge of the second external clock .

[c9] 7. The high speed data rate converting and switching circuit of claim 6, further comprising means to output data to the memory banks by latching the latching circuits by the rising and falling edges of the second external clock during a write operation.

[c10] 8. The high speed data rate converting and switching circuit of claim 7, further comprising means to produce a system bus strobe signal triggered by the rising edge of the second external clock during a write operation.

[c11] 9. A method for high speed data rate converting and switching for use in computer memory systems compris-

ing n memory banks, and further comprising a first external clock having a first frequency and a second external clock having a second frequency equal to n times the first frequency, the method comprising the steps of:
(d) Transferring each of a multiplicity of system bus data signals having the second frequency to a memory bank data signal having the first frequency during a write operation, and transfer each of a multiplicity of memory bank data signals having the first frequency to a system data bus data signal having the second frequency during a read operation in a data MUX and latch subsystem
(e) Generating a memory bank strobe signal having the first frequency, and which is synchronized to the memory bank data signals with a 90 degree phase shift during the write operation, generating a system bus strobe signal having the second frequency which is synchronized to, and in phase with, the system bus data signals during the read operation in a strobe MUX and latch subsystem.

[c12] (f) generating a memory bank mask signal having the first frequency, and is synchronized to the memory bank data signals during the write operation in a mask MUX and latch subsystem.

[c13] 10. The method of claim 9, further comprising:
(a) increasing the duration of each data bit during both

the read and the write operation by means of a multiplicity of latching circuits;
(b) generating an internal clock signal at the second frequency; and
(c) ANDing the internal clock signal with the output of each latching circuit,
so that the system bus data signal is at the second frequency.

[c14] 11. The method of claim 10, further comprising ANDing the first signal with the output of each latching circuit during the read operation,
so that the memory data bank signal is synchronized with the first external clock.

[c15] 12. The method of claim 11, wherein the generating of the internal clock signal at the second frequency further comprises using an m-bit counter.

[c16] 13. The method of claim 12, further comprising generating system strobe signals by ANDing a pull-up signal with the internal clock, and by ANDing a pull-down signal with the internal clock during the read operation.

[c17] 14. The method of claim 13, wherein the internal clock generating is accomplished by triggered by the falling edge of the second external clock .

[c18] 15. The method of claim 14, further comprising latching the latching circuits by the rising and falling edges of the second external clock during a write operation to output memory bank data signals.

[c19] 16. The method of claim 15, further comprising producing a system bus strobe signal triggered by the rising edge of the second external clock during a write operation.